REMARKS

Claims 1, 3, 4, and 14 have been amended. Claims 1-30 and 36-68 are pending in the present application. Applicant reserves the right to pursue the original claims and other claims in this application and in other applications.

Claims 1-29, 36-44, 50-59 and 65-68 stand rejected under 35 U.S.C. § 102 (e) as being anticipated by Leddige et al., US Patent No. 6,144,576 (hereinafter "Leddige"). The rejection is respectfully traversed and reconsideration is respectfully requested.

Claim 1 recites a method of routing a system bus to a plurality of expansion cards. The claim 1 method comprises the steps of "routing the bus into a first connector on a motherboard of the system and into a first circuit card residing within the first connector" and "routing the bus from a portion of the first circuit card into a portion of a second circuit card residing within a second connector on the motherboard." According to claim 1, "the bus is routed from the first circuit card to the second circuit card without entering the second connector." Applicant respectfully submits that Leddige does not disclose the claimed invention.

Leddige, by contrast, discloses a bus routing and wiring topology for a memory system 113 that routes a memory bus 300 from a controller 111 to socket connectors 220, 221, 223 located on the motherboard 200 of the system 113. "The motherboard 200 is a printed circuit board that interconnects components of the computer system 100 such as the bridge memory controller 111, the processor 101 and other components. The memory system 113 includes a plurality of memory modules 210-212. Each of the memory modules includes a plurality of memory devices mounted on the memory module." The memory modules 210-212 are insertable into the socket connectors 220-222. The socket connectors 220-222 are mounted on the motherboard 200. Leddige Col. 3, lines 35-48. Figure 2 of the Leddige patent is reproduced below.

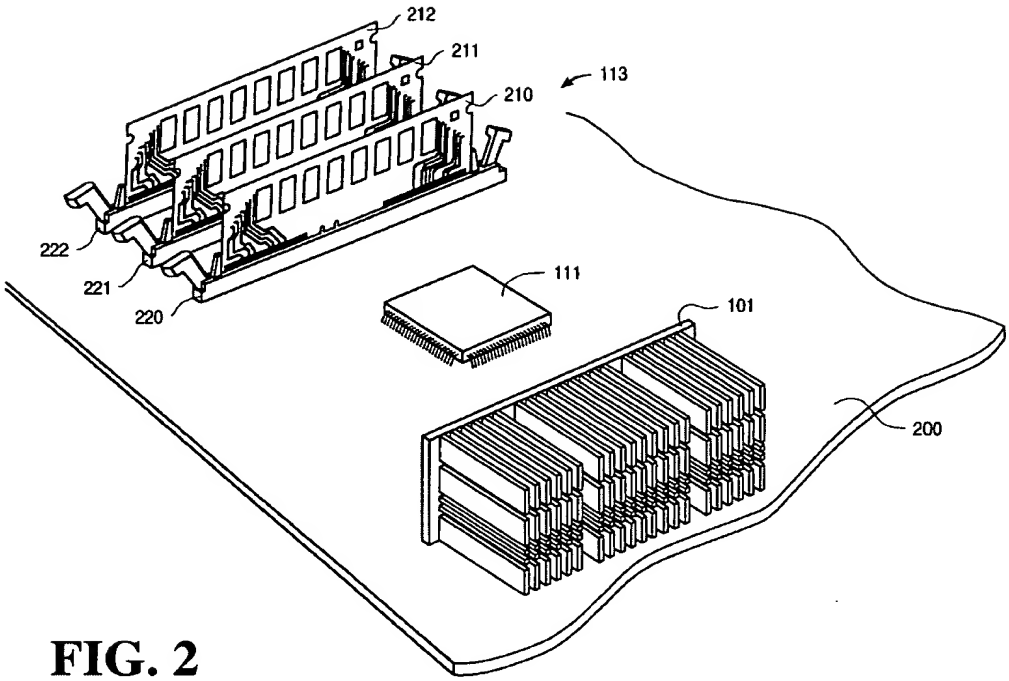

FIG. 2

Figure 2 of the Leddige Patent

According to Leddige,

> The memory bus 300 is a serial bus that is serially routed from the bridge memory controller 111 to the socket connectors 220-222. The memory bus 300 is routed from the first socket connector 220 to a first edge connector 310 on the first memory module 210. The memory bus 300 is routed from the first edge connector 310 to each of the memory devices on the first memory module 210 serially connecting each of the of memory devices on the first memory module 210. The memory bus 300 is routed from the last of the serially connected memory devices on the first memory module 210 to a second edge connector 311 on the memory module 210. From the second edge connector 311, the memory bus 300 is routed back to the first socket connector 220 and onto the second socket connector 221.
>
> Similarly, the memory bus 300 is routed from the second socket

> connector 221 onto a first edge connector 320 on the second memory module 211 and through a plurality of memory devices on the second memory module 211. The memory bus 300 serially connects each of the memory devices on the second memory module 211. The memory bus 300 is routed from the last of the serially connected memory devices on the second memory module 211 to a second edge connector 321 on the second memory module 211. The memory bus 300 is routed off the second edge connector 321 back to the second socket connector 221 and onto the third socket connector 222.
> Leddige Col. 3, line 62 to Col. 4, line 20 (emphasis added).

Thus, although Leddige routes the bus through the memory modules 210, 211, 212 (between edge connectors 310, 311 and 320, 321, etc.), Leddige does not disclose, teach or suggest the claimed invention for at least two reasons: (1) the Leddige memory bus 300 is routed from the first socket connector 220 to the second socket connector 221 (and from the second socket connector 221 to the third socket connector 222), whereas the claimed invention recites "routing the bus from a portion of the first circuit card into a portion of a second circuit card" and (2) the bus 300 is routed from the first socket connector 220 to the second socket connector 221 (and from the second socket connector 221 to the third socket connector 222) along the motherboard 200, whereas the claimed invention recites that "the bus is routed from the first circuit card to the second circuit card without entering the second connector."

These differences between the claimed invention and the Leddige system are reflected in circled portions of the figures that follow. In the claimed invention, the circled portion is not on the motherboard, whereas the circled portions in the Leddige system are on the motherboard 200 (as described above).

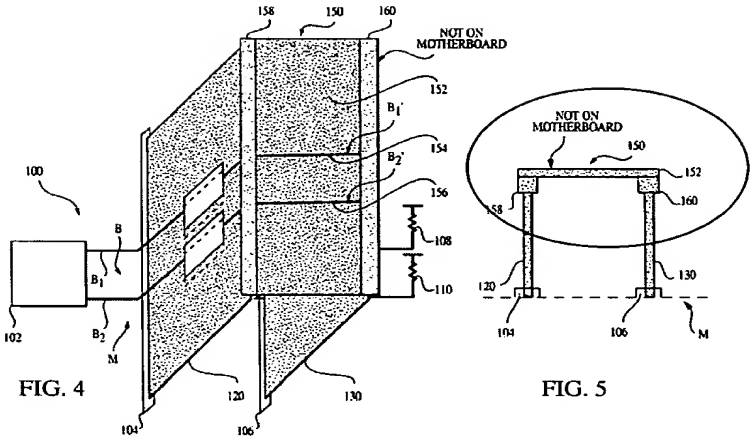

FIG. 4 FIG. 5

Figures 4 and 5 (one embodiment) of the claimed invention)

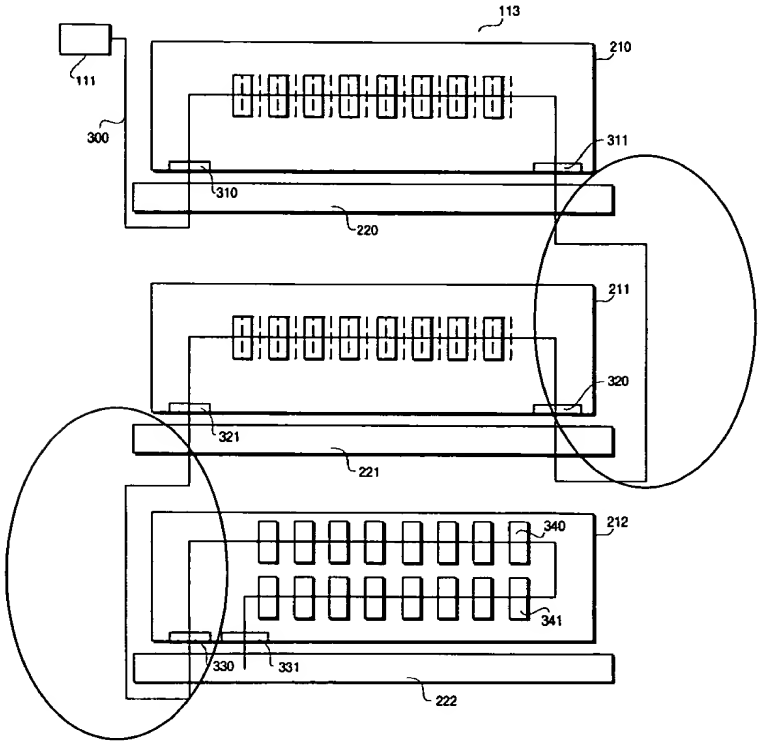

Figure 3 of the Leddige Patent

Another embodiment of the claimed invention is reproduced on the next page and is different from Leddige for at least the reasons set forth above (i.e., the circled portion is not on the mother board).

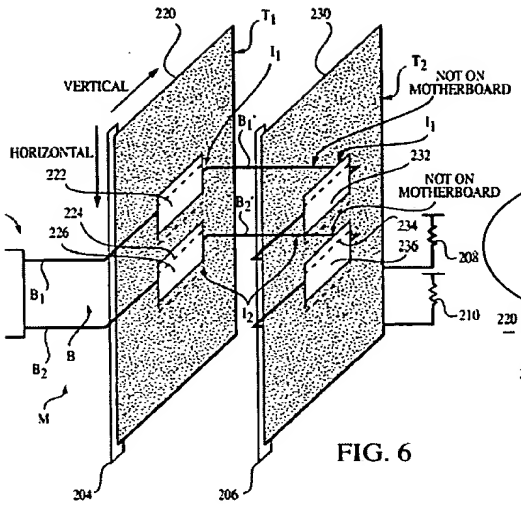

FIG. 6

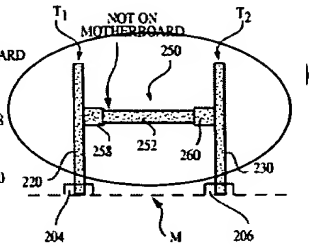

FIG. 7

FIGS. 6 and 7 (another embodiment of the claimed invention)

For at least the foregoing reasons, claim 1 is allowable over Leddige. Claims 1-13 depend from claim 1, and are allowable along with claim 1 for at least the reasons set forth above and on their own merits.

Claim 14 recites "routing the bus into a first circuit card residing within a first slot on the motherboard; routing the bus from a portion of the first circuit card into a portion of a second circuit card residing within a second slot on the motherboard, wherein the bus is routed from the first circuit card to the second circuit card without entering the second slot." As set forth above, Leddige fails to disclose these limitations. As such, claim 14 is allowable over Leddige. Claims 15-29 depend from claim 14, and are allowable along with claim 14 for at least the reasons set forth above and on their own merits.

Claim 36 recites "said bus is routed into a first connector, into a first circuit card residing within said first connector, out of a portion of said first circuit card into a portion of a second circuit card residing within a second connector and through said

second circuit card, and wherein said bus is routed from said first circuit card to said second circuit card without entering said second connector." As such, claim 36 is allowable over Leddige for at least the reasons set forth above. Claims 37-44 and 50 depend from claim 36, and are allowable along with claim 36 for at least the reasons set forth above and on their own merits.

Claim 51 recites "said bus is routed into a first circuit card residing within a first slot, out of a portion of said first circuit card and into a portion of a second circuit card residing within a second slot and out of the second circuit card, wherein said bus is routed from said first circuit card to said second circuit card without entering said second slot." As such, claim 51 is allowable over Leddige for at least the reasons set forth above. Claims 52-59 and 65 depend from claim 51, and are allowable along with claim 14 for at least the reasons set forth above and on their own merits.

Claim 66 recites "said bus is routed into a first connector, into a first circuit card residing within said first connector, out of a portion of said first circuit card into a portion of a second circuit card residing within a second connector, through said second circuit card and out of said second connector, wherein said bus is routed from said first circuit card into said second circuit card without entering said second connector." As such, claim 66 is allowable over Leddige for at least the reasons set forth above.

Claim 67 recites "said bus is routed into a first circuit card residing within a first slot, out of a portion of said first circuit card and into a portion of a second circuit card residing within a second slot and out of the second circuit card, wherein said bus is routed from said first circuit card into said second circuit card without entering said second slot." As such, claim 67 is allowable over Leddige for at least the reasons set forth above.

Claim 68 recites "wherein said bus is routed into a first memory circuit card residing within a first slot, out of a portion of said first memory circuit card and into a portion of a second memory circuit card residing within a second slot, and out of the second memory circuit card, wherein said bus is routed from said first memory circuit card into said second memory circuit card without entering said second slot." As such, claim 68 is allowable over Leddige for at least the reasons set forth above.

Accordingly, the rejection should be withdrawn and claims 1-29, 36-44, 50-59 and 65-68 allowed.

Claims 45 and 60 stand rejected under 35 U.S.C. § 103(a) as being obvious over Leddige in view of Cargin, Jr. et al., US. Patent. No. 6,023,147, (hereinafter "Cargin"). The rejection is respectfully traversed and reconsideration is respectfully requested.

Claim 45 depends from claim 36. As such, claim 45 recites "said bus is routed into a first connector, into a first circuit card residing within said first connector, out of a portion of said first circuit card into a portion of a second circuit card residing within a second connector and through said second circuit card, and wherein said bus is routed from said first circuit card to said second circuit card without entering said second connector." Claim 60 depends from claim 51 and recites "said bus is routed into a first circuit card residing within a first slot, out of a portion of said first circuit card and into a portion of a second circuit card residing within a second slot and out of the second circuit card, wherein said bus is routed from said first circuit card to said second circuit card without entering said second slot."

As noted above, Leddige fails to disclose, teach or suggest these limitations. Applicant respectfully submits that Cargin, which merely teaches a cable, fails to teach

or suggest the limitations that are missing in Leddige. As such, claims 45 and 60 are allowable over the cited combination for at least the reasons set forth above and on their own merits. The rejection should be withdrawn and the claims allowed.

Claims 46-49 and 61-64 stand rejected under 35 U.S.C. § 103(a) as being obvious over Leddige in view of the Handbook of LAN Cable Testing (hereinafter the "Handbook"). The rejection is respectfully traversed and reconsideration is respectfully requested.

Claims 46-49 depend from claim 36. As such, the claims recite "said bus is routed into a first connector, into a first circuit card residing within said first connector, out of a portion of said first circuit card into a portion of a second circuit card residing within a second connector and through said second circuit card, and wherein said bus is routed from said first circuit card to said second circuit card without entering said second connector." Claims 61-64 depend from claim 51 and recite "said bus is routed into a first circuit card residing within a first slot, out of a portion of said first circuit card and into a portion of a second circuit card residing within a second slot and out of the second circuit card, wherein said bus is routed from said first circuit card to said second circuit card without entering said second slot."

As noted above, Leddige fails to disclose, teach or suggest these limitations. Applicant respectfully submits that the Handbook, which merely teaches cable types, fails to teach or suggest the limitations that are missing in Leddige. As such, claims 46-49 and 61-64 are allowable over the cited combination for at least the reasons set forth above and on their own merits. The rejection should be withdrawn and the claims allowed.

Claims 3 and 4 were not amended for purposes of patentability.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
Gianni Minutoli
Registration No.: 41,198
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant